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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,256	O'CONNOR ET AL.	
	Examiner	Art Unit	
	James Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-30 and 34-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Bose et al. (U.S. Patent Publication No. 2004/0221185 A1) (hereinafter referred to as Bose).

As to claim 1, Bose discloses a method comprising: initiating a power increase for a potentially needed functional unit to an operable power level (Bose discloses a signal [134] sent from a unit-level activity prediction logic [130] to target execution units [118, 120, 122, et al.] to change from a "sleep" or "power-down" state to a "wake up" state; paragraph 37, lines 20-28 and paragraph 38), if the potentially needed functional unit has a present power level that is lower than the operable power level, wherein the potentially needed functional unit is identified based on a determination of whether the potentially needed functional unit is operable to execute at least one software instruction stored within an instruction cache (Bose discloses the prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 2, Bose discloses the method further comprising: fetching one or more software instructions into the instruction cache engine (Bose discloses machine instructions

being fetched from an instruction cache but, as is known in the art, said instructions are originally fetched from system memory into the instruction cache of a processor and essentially made available to a processing engine [instruction decode-dispatch unit IDU 114] for execution; paragraph 39, lines 1-24).

As to claim 3, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a conventional cache (paragraph 37).

As to claim 4, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a trace cache (As it is known in the art, a trace cache performs the task of performing repeat instructions that have been branched or follow the path of instructions as needed which is what the cache [102] of Bose performs; paragraphs 37 and 39).

As to claim 5, Bose discloses the method further comprising: fetching a line of one or more software instructions into the instruction cache (Bose discloses machine instructions being fetched from an instruction cache but, as is known in the art, said instructions are originally fetched from system memory into the instruction cache of a processor and essentially made available to a processing engine [instruction decode-dispatch unit IDU 114] for execution; paragraph 39, lines 1-24); generating and storing an information vector (132) for the line, wherein the information vector identifies a set of functional units that are operable to execute the one or more software instructions (paragraph 42); and identifying the potentially needed functional unit based on the information vector (with request signals 134; paragraph 40).

As to claim 6, Bose discloses the method further comprising: indicating (signaling) power status information (via signal 134) for a set of functional units (paragraph 40), wherein the

power status information indicates whether a functional unit, within the set of functional units, has a present power level that places the functional unit in an operable power state or a low power state (paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 7, Bose discloses the method further comprising: incrementing a use counter (168) for a functional unit when a software instruction is fetched into the instruction cache, and when the functional unit is operable to execute at least part of the software instruction (paragraphs 46 and 51).

As to claim 8, Bose discloses the method further comprising: decrementing the use counter (168) for the functional unit when the software instruction is eliminated from the instruction cache (paragraph 46 and 50).

As to claim 9, Bose discloses the method further comprising: selecting one or more selected lines of software instructions stored within the cache (paragraph 39, lines 1-3); and identifying (predicting) the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within the one or more selected lines (paragraph 39, lines 3-24 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 10, Bose discloses the method further comprising: activating (fetching and processing) a line of software instructions stored within the cache (paragraph 39, lines 1-24); and identifying (predicting) the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within the line (paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 11, Bose discloses the method further comprising: identifying (predicting) an unneeded functional unit as a functional unit that is not operable to execute the at least one

software instruction (paragraph 40, line 1 thru paragraph 41, line 5); and initiating (signaling via signal 134) a power decrease for the unneeded functional unit, if the unneeded functional unit has a second present power level that is greater than or equal to a second operable power level (paragraphs 39-40 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 12, Bose discloses the method wherein initiating the power decrease comprises: initiating (signaling via signal 134) the power decrease for the unneeded functional unit after execution is complete of any in-flight instructions (branched) that use the unneeded functional unit (paragraph 37, lines 20-28 and paragraph 42).

As to claim 13, Bose discloses the method wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

As to claim 14, Bose discloses the method wherein initiating the power increase comprises: determining a selected operable power level from one of multiple operable power levels ("sleep," "power-down" or "wake up"), wherein the selected operable power level is selected based on an expected result latency; and initiating the power increase to the selected operable power level (paragraphs 28 and 42).

As to claim 15, Bose discloses a method comprising: fetching one or more lines of software instructions into an instruction cache (ICACHE 102), which is accessible to a processing engine (instruction decode-dispatch unit IDU 114) (Bose discloses machine

instructions being fetched from an instruction cache but, as is known in the art, said instructions are originally fetched from system memory into the instruction cache of a processor and essentially made available to a processing engine [instruction decode-dispatch unit IDU 114] for execution; paragraph 39, lines 1-24); identifying (predicting) potentially needed functional units as functional units that are operable to execute at least one software instruction stored within the instruction cache (Bose discloses the prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5 and paragraph 42), wherein a functional unit includes a portion of hardware (118, 120, 122, et al.), which is operable to perform a function in response to special instructions received from the processing engine (paragraph 39, lines 17-24); identifying (predicting) unneeded functional units as functional units that are not operable to execute a software instruction stored within the instruction cache (paragraph 41, lines 1-8 and paragraph 42); initiating a power increase ("wake up" signal via signal 134 from the prediction unit 130) for selected ones of the potentially needed functional units that are in a low power state (paragraph 37, lines 20-28); and initiating a power decrease ("sleep" or "power-down" signal via signal 134 from the prediction unit 130) for selected ones of the unneeded functional units that are in an operable power state (paragraph 37, lines 20-28).

As to claim 16, Bose discloses the method further comprising: generating and storing (concatenated from the instruction fetch address register IFAR field) an information vector (132) for selected ones of the one or more lines, wherein the information vector identifies a set of functional units that are operable to execute software instructions within a line; and wherein identifying the potentially needed functional unit is performed based on the information vector (paragraph 42).

As to claim 17, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a conventional cache (paragraph 37).

As to claim 18, Bose discloses the method wherein fetching the one or more instructions comprises fetching the one or more instructions into a trace cache (As it is known in the art, a trace cache performs the task of performing repeat instructions that have been branched or follow the path of instructions as needed which is what the cache [102] of Bose performs; paragraphs 37 and 39).

As to claim 19, Bose discloses the method wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

As to claim 20, Bose discloses the method wherein initiating the power increase comprises: determining a selected operable power level from one of multiple operable power levels ("sleep," "power-down" or "wake up"), wherein the selected operable power level is selected based on an expected result latency; and initiating the power increase to the selected operable power level (paragraphs 28 and 42).

As to claim 21, Bose discloses a computer-readable medium having program instructions stored thereon to perform a method, which when executed within an electronic system, results in: identifying (predicting) a potentially needed functional unit as a functional unit that is operable to execute at least one software instruction stored within an instruction cache (Bose discloses the

prediction logic [130] determining if execution units are needed; paragraph 40, line 1 thru paragraph 41, line 5 and paragraph 42); and initiating a power increase ("wake up" signal via signal 134 from the prediction unit 130) for the potentially needed functional unit (118, 120, 122, et al.), if the potentially needed functional unit has a present power level that is lower than an operable power level (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 22, Bose discloses the computer-readable medium wherein executing the program instructions further results in: fetching a line of one or more software instructions into the instruction cache (Bose discloses machine instructions being fetched from an instruction cache but, as is known in the art, said instructions are originally fetched from system memory into the instruction cache of a processor and essentially made available to a processing engine [instruction decode-dispatch unit IDU 114] for execution; paragraph 39, lines 1-24); generating and storing (concatenated from the instruction fetch address register IFAR field) an information vector (132) for the line, wherein the information vector identifies a set of functional units that are operable to execute the one or more software instructions; and wherein identifying the potentially needed functional unit is performed based on the information vector (paragraph 42).

As to claim 23, Bose discloses the computer-readable medium wherein executing the program instructions further results in: selecting one or more selected lines of software instructions stored within the cache (paragraph 39, lines 1-3); and wherein identifying (predicting) the potentially needed functional unit includes identifying the potentially needed functional unit as a functional unit that is operable to execute at least one software instruction

stored within the one or more selected lines (paragraph 39, lines 3-24 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 24, Bose discloses the computer-readable medium wherein executing the program instructions further results in: identifying (predicting) an unneeded functional unit as a functional unit that is not operable to execute the at least one software instruction (paragraph 40, line 1 thru paragraph 41, line 5); and initiating (signaling via signal 134) a power decrease for the unneeded functional unit, if the unneeded functional unit has a second present power level that is greater than or equal to a second operable power level (paragraphs 39-40 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 25, Bose discloses the computer-readable medium wherein initiating the power increase comprises: initiating (signaling via signal 134) the power increase for a functional unit selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

As to claim 26, Bose discloses an apparatus comprising: one or more functional units (execution units 118, 120, 122); an instruction cache (ICACHE 102); a processing engine (instruction decode-dispatch unit IDU 114), which is operable to access software instructions stored within the instruction cache (via buffer 106), and send one or more special instructions to the one or more functional units in order to execute at least some of the software instructions (via issue queue 116) (Bose discloses instructions being fetched from instruction cache [102] to a buffer [106] then to the processing engine [IDU 114] and nest an issue queue [116] to be

processed by execution units [118, 120 or 122]; paragraph 36, lines 1-24); and one or more power controllers (unit-level activity prediction logic 130), which are operable to control (send "sleep," "power-down," or "wake up" signals via 134) whether or not an (predicting) operable power level or a low power level is provided to selected ones of the one or more functional units (paragraph 40), based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

As to claim 27, Bose discloses the apparatus wherein at least one of the one or more functional units includes an internal functional unit, which is located on a same chip as the processing engine (Bose discloses the processor being a pipelined processor such that the functional units will contain multiple stage units for processing; paragraphs 37 and 62).

As to claim 28, Bose discloses the apparatus wherein at least one of the one or more functional units includes an external functional unit, which is not located on a same chip as the processing engine (Any other unit used for processing not found within the processing engine [IDU 114]; paragraph 37).

As to claim 29, Bose discloses the apparatus wherein the instruction cache includes a conventional cache (paragraph 37).

As to claim 30, Bose discloses the apparatus wherein the instruction cache includes a trace cache (As it is known in the art, a trace cache performs the task of performing repeat instructions that have been branched or follow the path of instructions as needed which is what the cache [102] of Bose performs; paragraphs 37 and 39).

As to claim 34, Bose discloses the apparatus further comprising: a predecoder (part of IDU 114), which is operable to evaluate selected ones of the software instructions to determine which functional units will be needed to execute an instruction (paragraph 42).

As to claim 35, Bose discloses the apparatus further comprising: a battery interface, operable to provide power to the one or more functional units (paragraph 6).

As to claim 36, Bose discloses the apparatus further comprising: a wireless medium interface, operable to enable signals to be sent to and received over a wireless medium (Bose discloses laptops, portable and mobile systems that commonly have wireless medium interfaces as is known in the art; paragraph 6).

As to claim 37, Bose discloses the apparatus further comprising: a network interface, operable to enable signals to be sent to and received from a network (Bose discloses laptops, portable and mobile systems that commonly have network interfaces as is known in the art; paragraph 6).

As to claim 38, Bose discloses the apparatus wherein the one or more functional units comprise: one or more functional units selected from a group of functional units that includes one or more floating-point units, multipliers, dividers, shifters, digital signal processors, co-processors, application specific integrated circuits, data processing engines, debug logic blocks, encryption units and key-generation units (paragraph 37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-33 and 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bose et al. (U.S. Patent Publication No. 2004/0221185 A1) (hereinafter referred to as Bose) in view of Theis (U.S. Patent Publication No. 2005/0251621 A1) (hereinafter referred to as Theis).

As to claim 31, Bose discloses an instruction cache (ICACHE 102) but does not discloses the instruction cache comprises: an array of storage locations; and a mechanism to sequentially access the storage locations within the array using an enable signal, which has a value that results from shifting information within one or more shift registers.

Theis teaches a memory within a processor (instruction cache; paragraph 4, lines 1-9 and paragraph 22, lines 15-19 and paragraphs 85-86) that contains an array (stack) of storage locations (addresses) that sequentially accesses (circular stack which sequentially accesses said addresses) using an enable signal (symbolic variables specified) that accesses the stack which has a value (stack pointer value) that results from shifting within one or more shift registers (paragraphs 191, 192 and 218). Theis also has the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

It would have been obvious to one of ordinary skill of the art having the teachings of Bose and Theis at the time the invention was made, to modify the instruction cache of Bose to include the ability to store and access an array (stack) of addresses sequentially by use of shift registers as taught by Theis. One of ordinary skill in the art would be motivated to make this combination of having an instruction cache that can store and access an array (stack) of addresses sequentially by use of shift registers in view of the teachings of Theis, as doing so

would give the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

As to claim 32, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of first latches, within which a first portion of the enable signal is stored, and wherein the first portion of the enable signal is used to activate a selected word line within the array (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which as is known in the art uses a latch [multiplexor] to select the stack item; paragraph 218).

As to claim 33, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of second latches, within which a second portion of the enable signal is stored, wherein the second portion of the enable signal is used to select a portion of the selected word line (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which as is known in the art uses a latch [multiplexor] to select the stack item; paragraph 218).

As to claim 39, Bose discloses an apparatus comprising: one or more functional units (execution units 118, 120, 122); an instruction cache (ICACHE 102); a processing engine (instruction decode-dispatch unit IDU 114), which is operable to access software instructions stored within the instruction cache (via buffer 106), and send one or more special instructions to the one or more functional units in order to execute at least some of the software instructions (via issue queue 116) (Bose discloses instructions being fetched from instruction cache [102] to a buffer [106] then to the processing engine [IDU 114] and nest an issue queue [116] to be processed by execution units [118, 120 or 122]; paragraph 36, lines 1-24).

Bose fails to disclose said instruction cache including an array of storage locations, and a mechanism to sequentially access the storage locations within the array using an enable signal, which has a value that results from shifting information within one or more shift registers.

Theis teaches a memory within a processor (instruction cache; paragraph 4, lines 1-9 and paragraph 22, lines 15-19 and paragraphs 85-86) that contains an array (stack) of storage locations (addresses) that sequentially accesses (circular stack which sequentially accesses said addresses) using an enable signal (symbolic variables specified) that accesses the stack which has a value (stack pointer value) that results from shifting within one or more shift registers (paragraphs 191, 192 and 218). Theis also has the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

It would have been obvious to one of ordinary skill of the art having the teachings of Bose and Theis at the time the invention was made, to modify the instruction cache of Bose to include the ability to store and access an array (stack) of addresses sequentially by use of shift registers as taught by Theis. One of ordinary skill in the art would be motivated to make this combination of having an instruction cache that can store and access an array (stack) of addresses sequentially by use of shift registers in view of the teachings of Theis, as doing so would give the added benefit of accessing addresses using both conventional machine code as high level programming languages (paragraphs 78-81).

As to claim 40, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of first latches, within which a first portion of the enable signal is stored, and wherein the first portion of the enable signal is used to activate a selected word line within the array (Theis teaches the stack of addresses being sequentially accessed by

use of a stack pointer which as is known in the art uses a latch [multiplexor] to select the stack item; paragraph 218).

As to claim 41, Theis teaches the apparatus wherein the mechanism to sequentially access the storage locations includes a plurality of second latches, within which a second portion of the enable signal is stored, wherein the second portion of the enable signal is used to select a portion of the selected word line (Theis teaches the stack of addresses being sequentially accessed by use of a stack pointer which as is known in the art uses a latch [multiplexor] to select the stack item; paragraph 218).

As to claim 42, Bose discloses the apparatus further comprising: one or more power controllers (unit-level activity prediction logic 130), which are operable to control (send "sleep," "power-down," or "wake up" signals via 134) whether or not an operable power level or a low power level is provided to selected ones of the one or more functional units (paragraph 40), based on whether or not selected ones of the one or more functional units are operable to execute at least one software instruction stored within the instruction cache (paragraph 37, lines 20-28 and paragraph 40, line 1 thru paragraph 41, line 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
Patent Examiner, Art Unit 2116
April 14, 2006